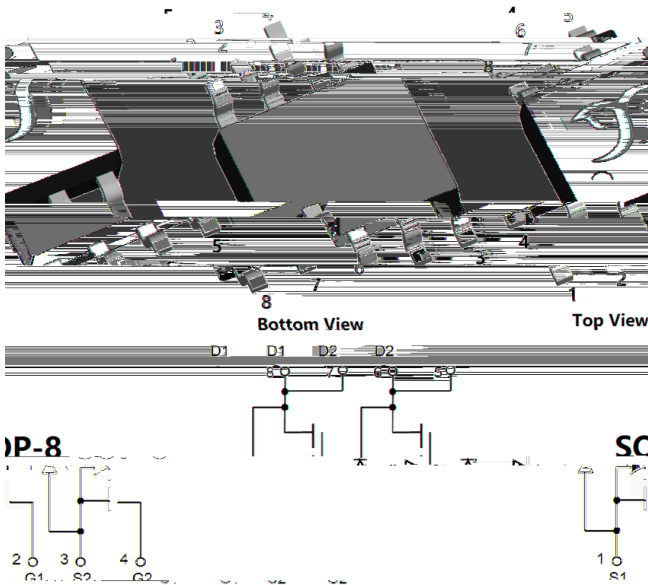




N-Channel and N-Channel Complementary MOSFET



Product Summary

V_{DS}	40V
I_D	7A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	$<32m$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	$<50m$
100% EAS Tested	

General Description

Trench Power MV MOSFET technology
High Speed switching

Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

Power switching application
Uninterruptible power supply
Load switch

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^{\circ}C$	I_D	7	A
	$T_A=100^{\circ}C$		4	
Pulsed Drain Current ^A		I_{DM}	30	A
Avalanche energy ^B		EAS	14	mJ
Total Power Dissipation ^C	$T_A=25^{\circ}C$	P_D	2	W
	$T_A=100^{\circ}C$		0.8	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$^{\circ}C$

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R	50	60	$^{\circ}C/W$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJSD07N04B	F2	Q07N04B	4000	8000	64000	reel



YJSD07N04B

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	
		$V_{DS}=40V, V_{GS}=0V, T_J=150^{\circ}\text{C}$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$					



Typical Electrical and Thermal Characteristics Diagrams

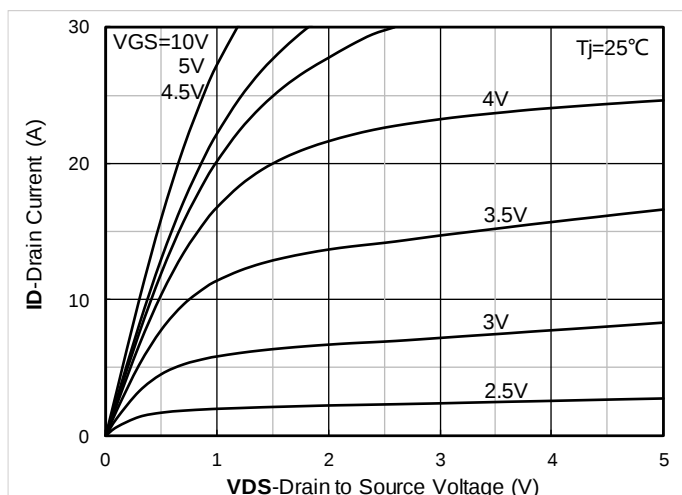


Figure 1. Output Characteristics

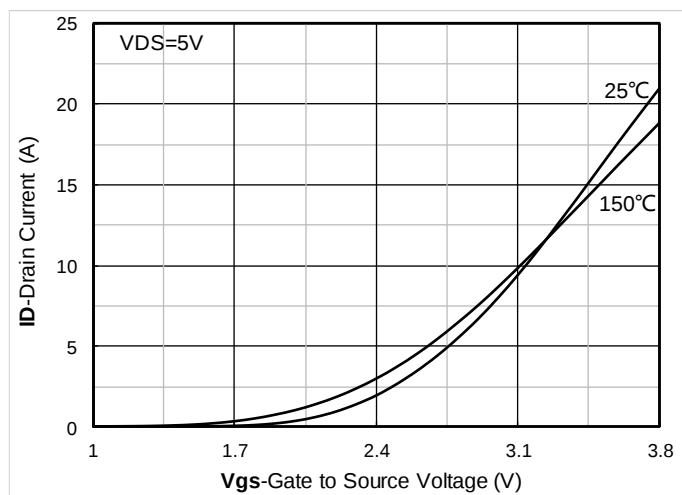


Figure 2. Transfer Characteristics

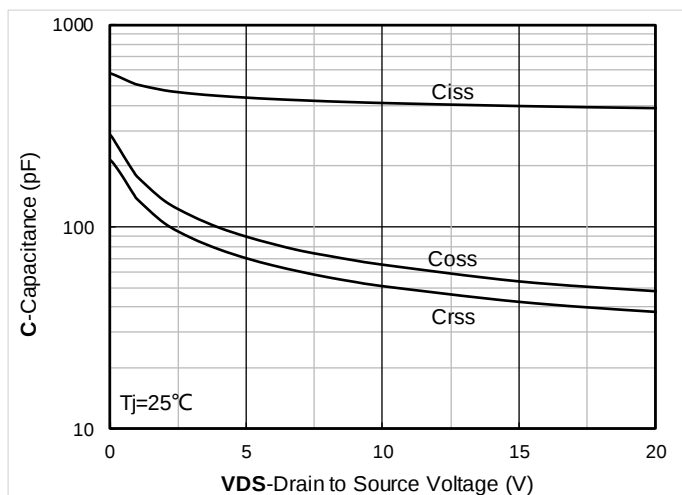


Figure 3. Capacitance Characteristics

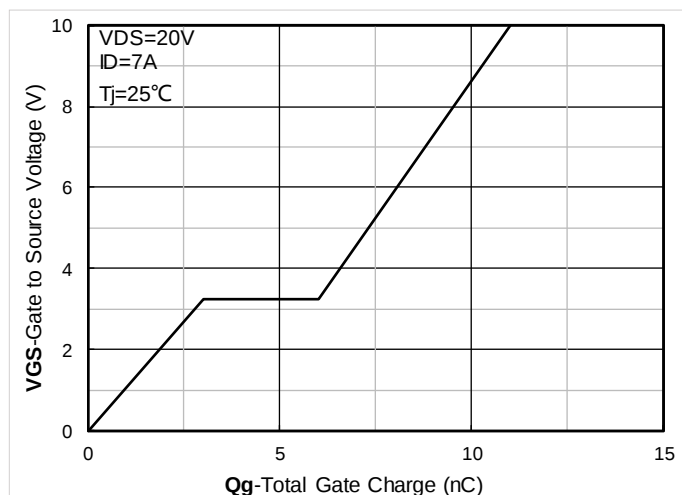


Figure 4. Gate Charge

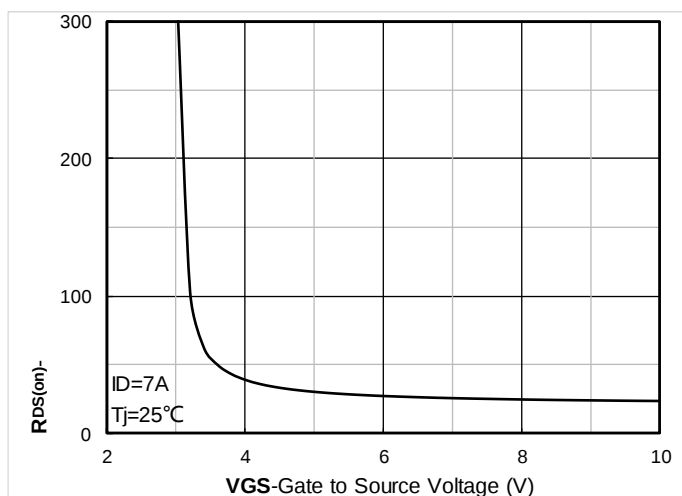


Figure 5. On-Resistance vs Gate to Source Voltage

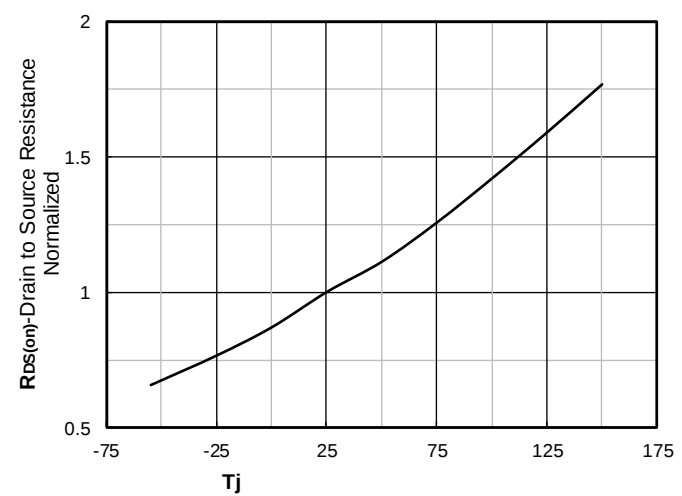


Figure 6. Normalized On-Resistance

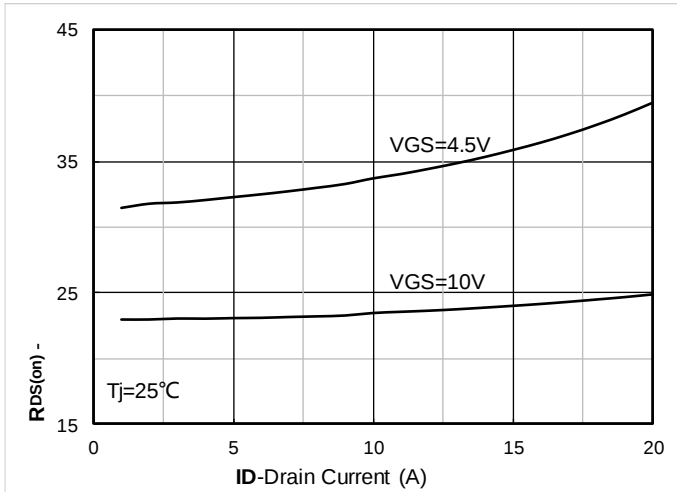


Figure 7. $R_{DS(on)}$ VS Drain Current

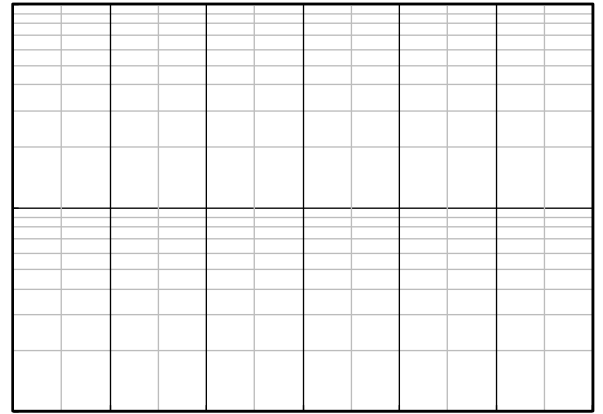


Figure 8. Forward characteristics of reverse diode

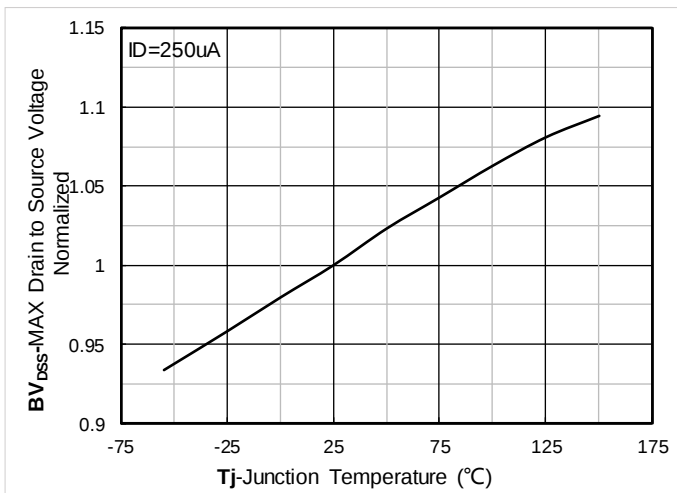


Figure 9. Normalized breakdown voltage

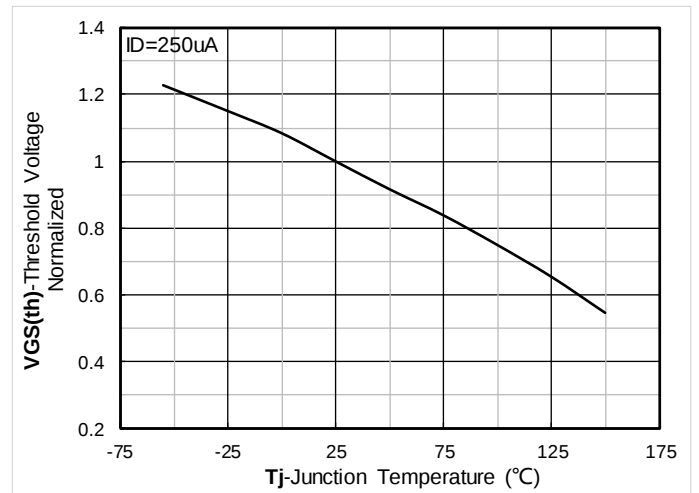


Figure 10. Normalized Threshold voltage

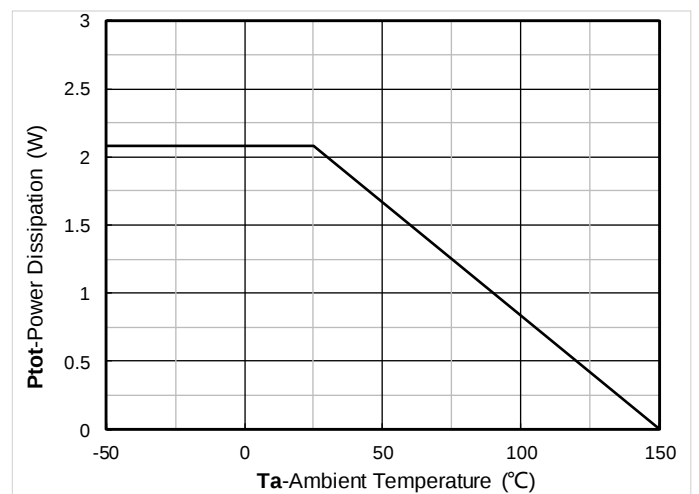


Figure 11. Current dissipation

Figure 12. Power dissipation

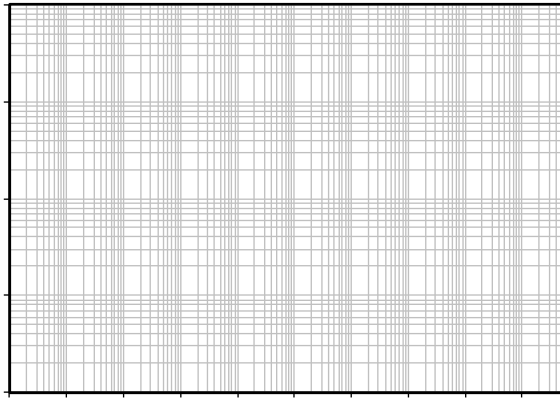


Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

Test Circuits & Waveforms

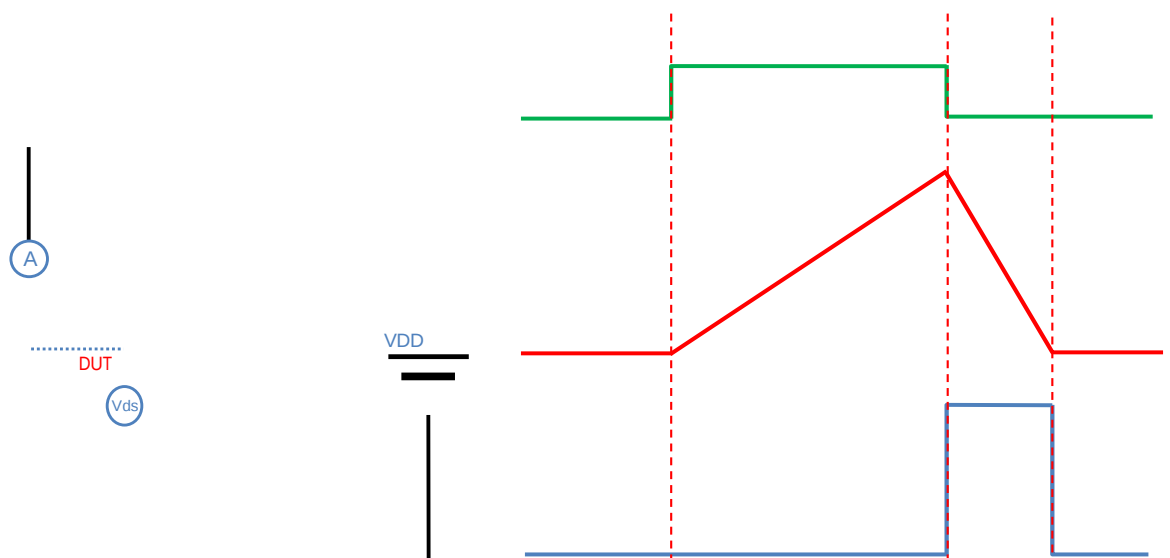


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

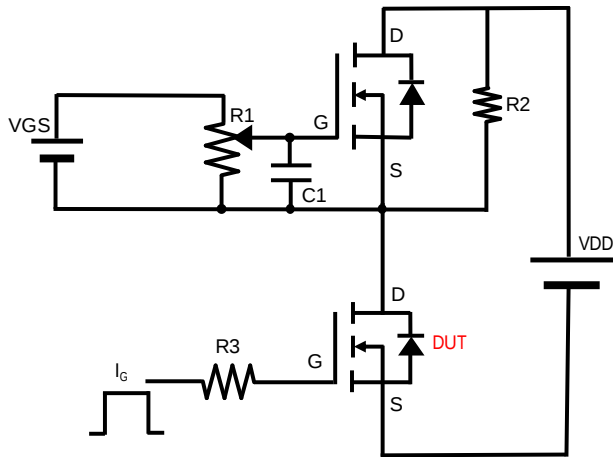


Figure B. Gate Charge Test Circuit & Waveform

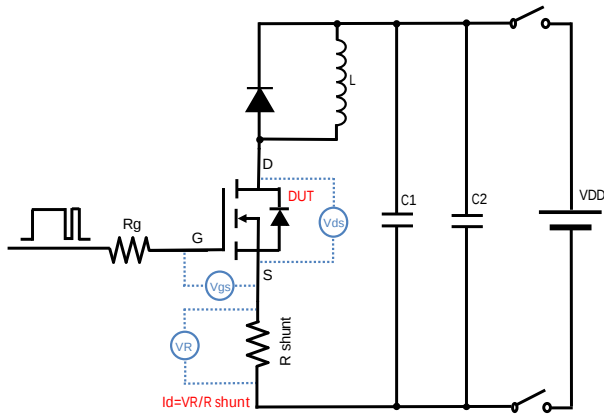


Figure C. Resistive Switching Test Circuit & Waveform

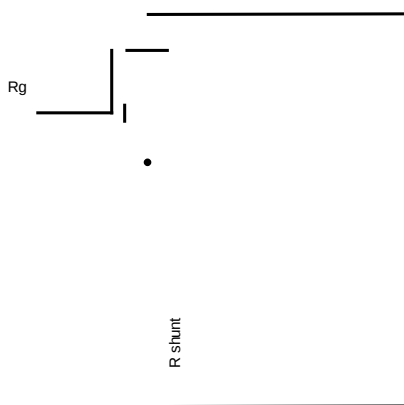


Figure D. Diode Test Circuit & Waveform



SOP8 Package information

B			
D		0.020	
E			
F			
	0.050		
H			
J			
K			



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