

YJS3404B

and N-Channel Complementary MOSFET

Product Summary

V_{DS}	30V
I_D	6.5A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	<20m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<41m

General Description

Trench Power LV MOSFET technology
High density cell design for low $R_{DS(ON)}$
High Speed switching
3
-0 Flammability Rating
alogen Free

Applications

Battery protection
Load switch
Power management

$T_A=25^{\circ}C$ unless otherwise noted)

		Symbol	Limit	Unit
		V_{DS}	30	V
		V_{GS}	± 20	V
ate	$T_A=25^{\circ}C$	I_D	6.5	A
	$T_A=100^{\circ}C$		4.1	
	$T_A=25^{\circ}C$		8.5	
	$T_A=100^{\circ}C$		5.3	
		I_{DM}	50	A
ate	$T_A=25^{\circ}C$	P_D	1.25	W
	$T_A=100^{\circ}C$		0.5	
	$T_A=25^{\circ}C$		1.92	
	$T_A=100^{\circ}C$		0.76	
		T_J, T_{STG}	-55~+150	$^{\circ}C$

	Symbol	Typ	Max	Units
Steady-State	R	80	100	$^{\circ}C/W$



YJS3404B

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	
		$V_{DS}=30V, V_{GS}=0V, T_J=150^{\circ}\text{C}$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D$	1	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=6.5A$	-	15.5	20	



Typical Electrical and Thermal Characteristics Diagrams

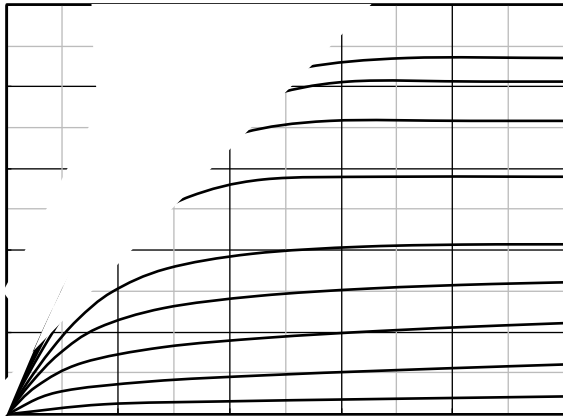


Figure 1. Output Characteristics

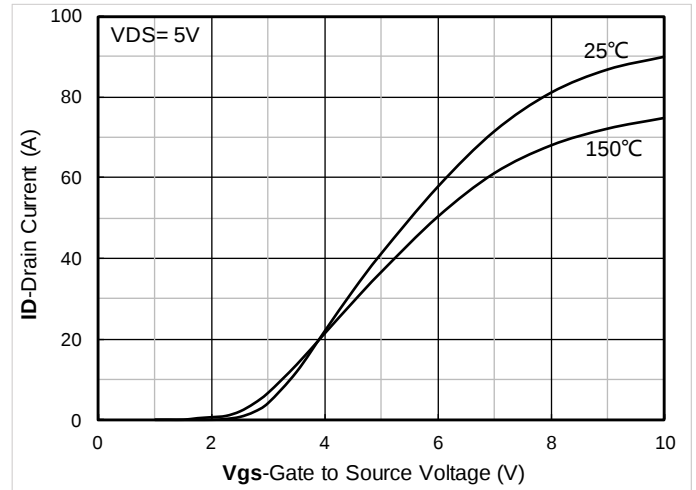


Figure 2. Transfer Characteristics

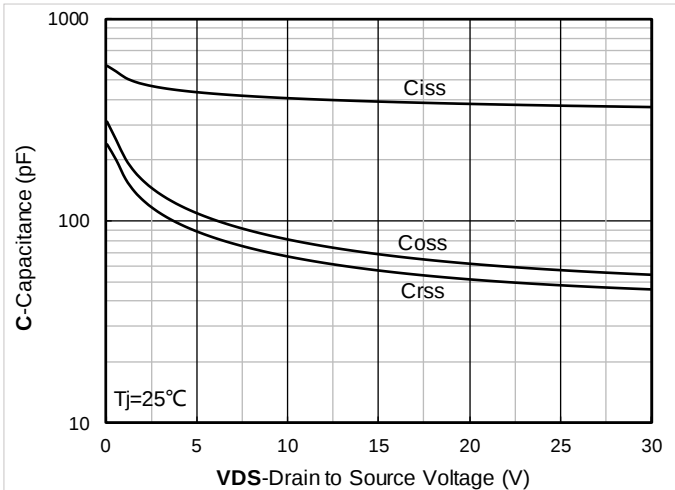


Figure 3. Capacitance Characteristics

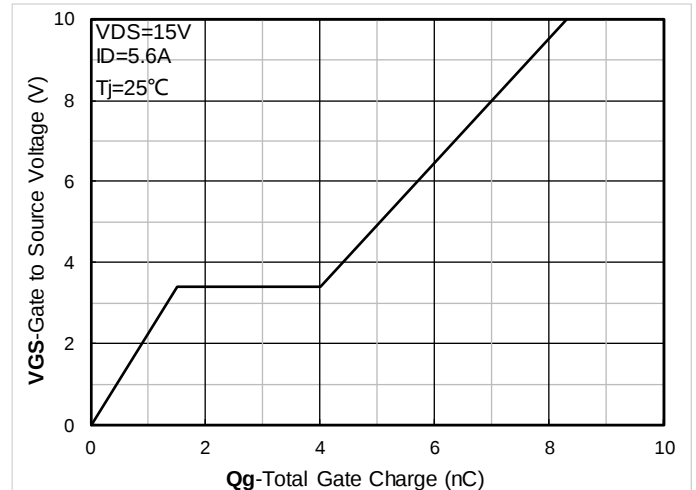


Figure 4. Gate Charge

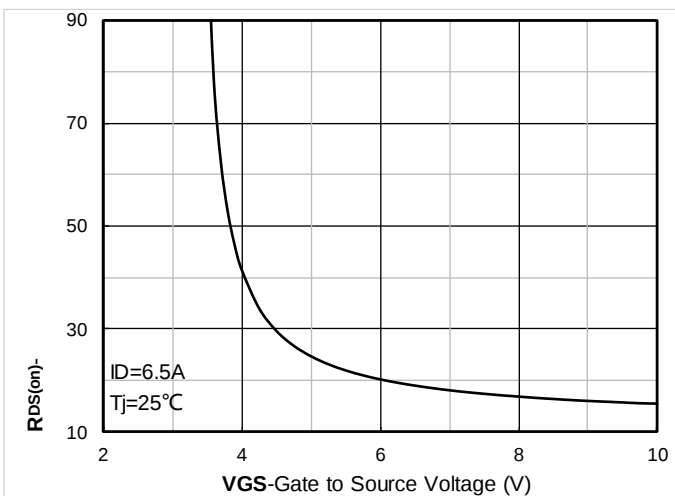


Figure 5. On-Resistance vs. Gate to Source Voltage

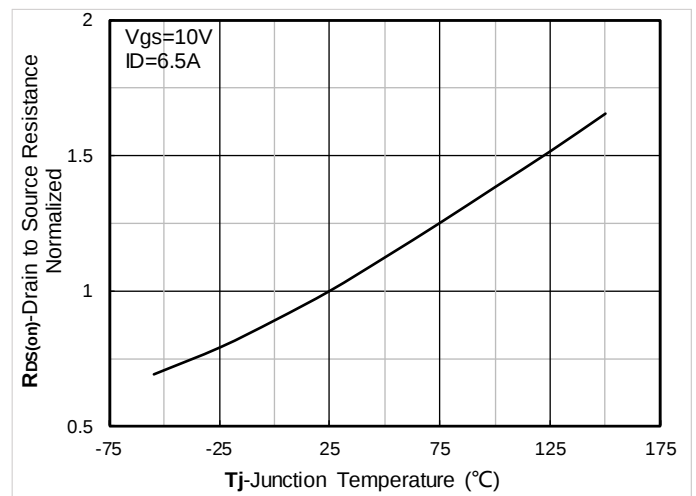


Figure 6. Normalized On-Resistance

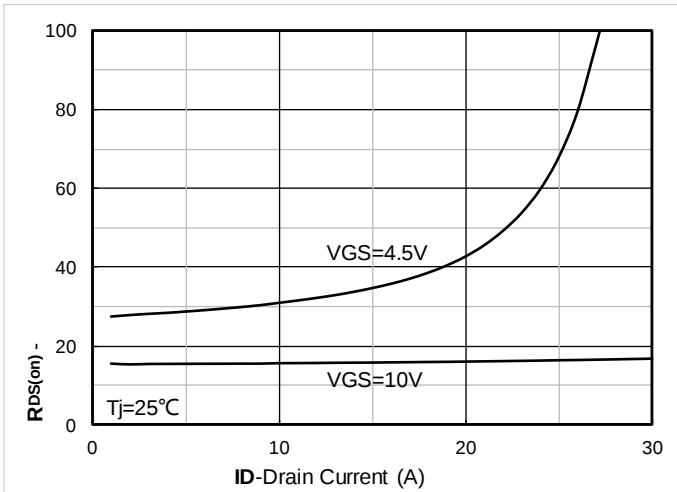


Figure 7. $R_{DS(on)}$ VS Drain Current

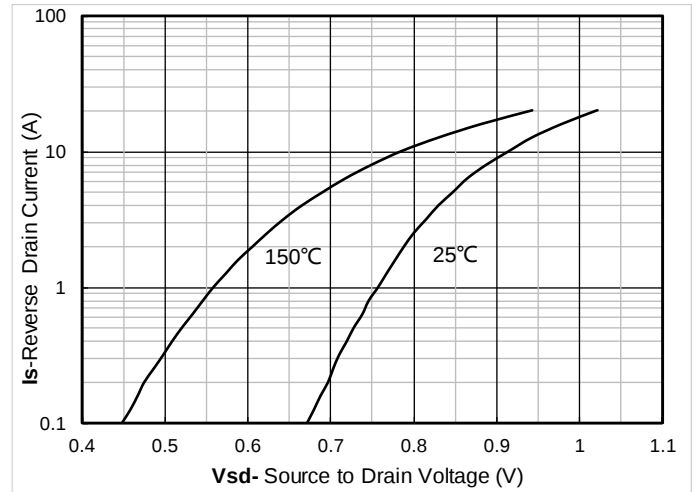


Figure 8. Forward characteristics of reverse diode

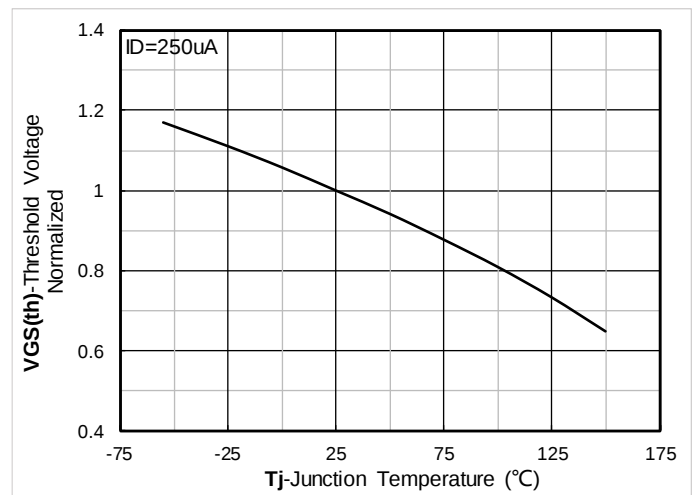


Figure 9. Normalized breakdown voltage

Figure 10. Normalized Threshold voltage

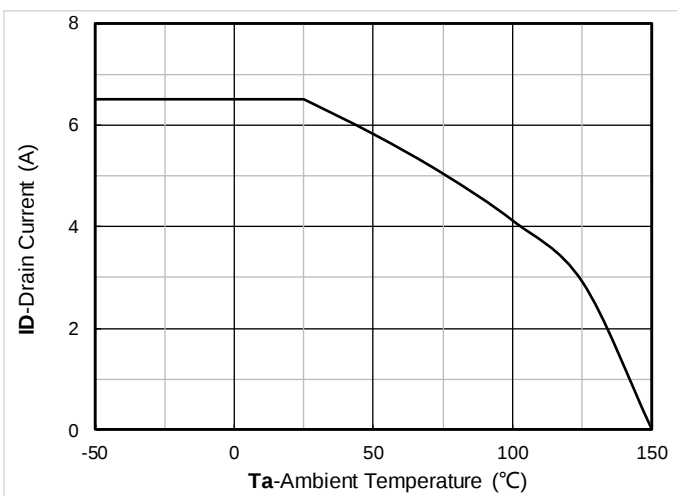


Figure 11. Current dissipation

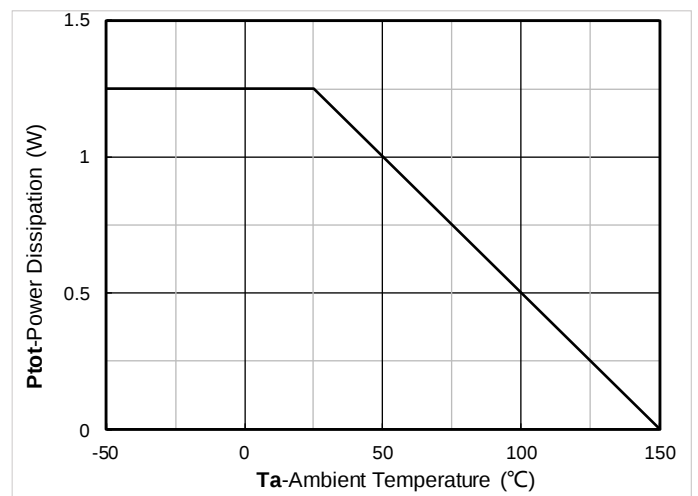


Figure 12. Power dissipation

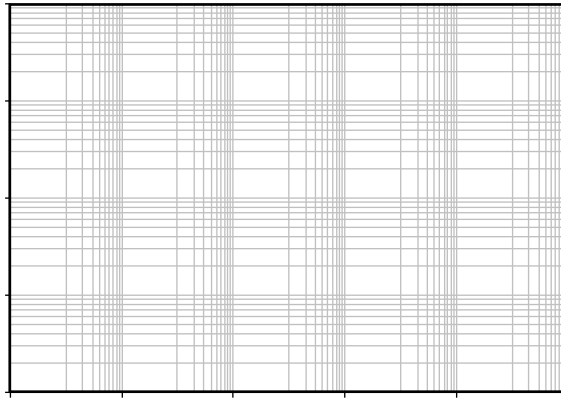


Figure 13. Maximum Transient Thermal Impedance

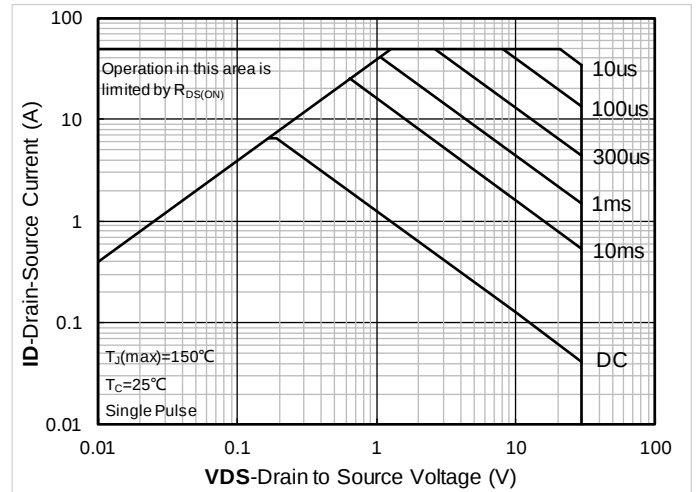


Figure 14. Safe Operation Area

Test Circuits & Waveforms

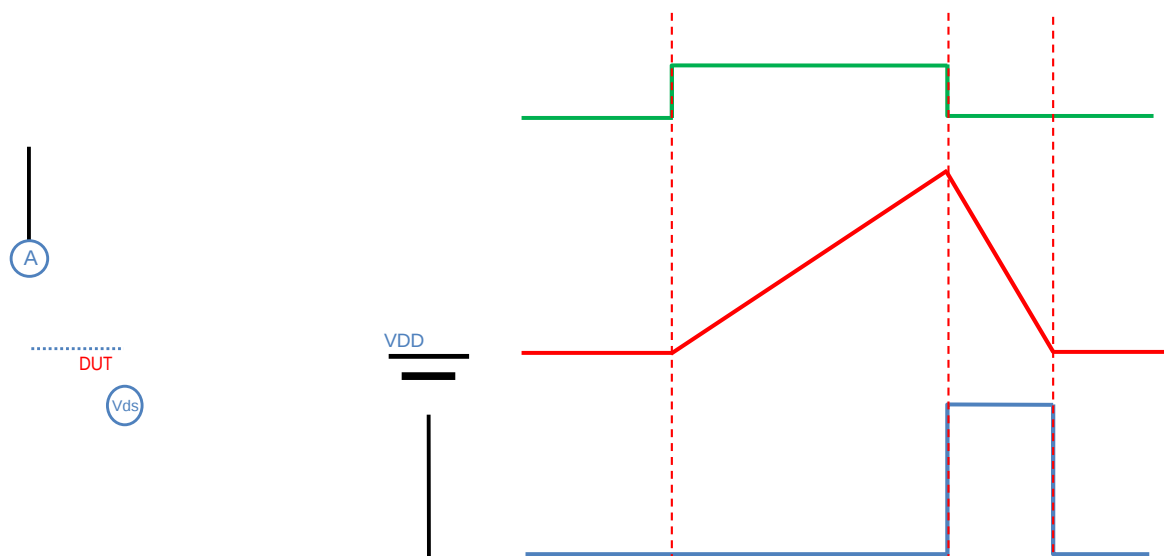


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

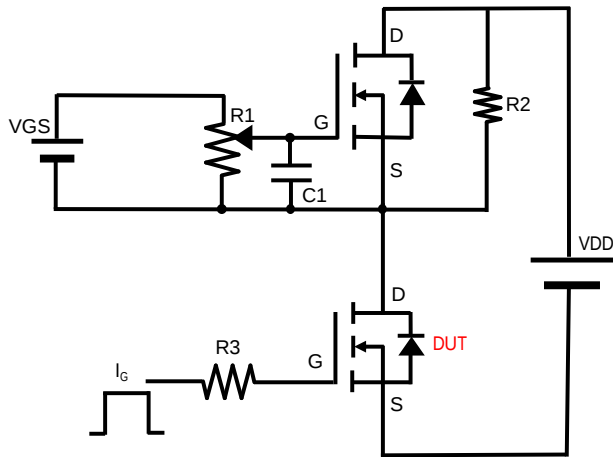


Figure B. Gate Charge Test Circuit & Waveform

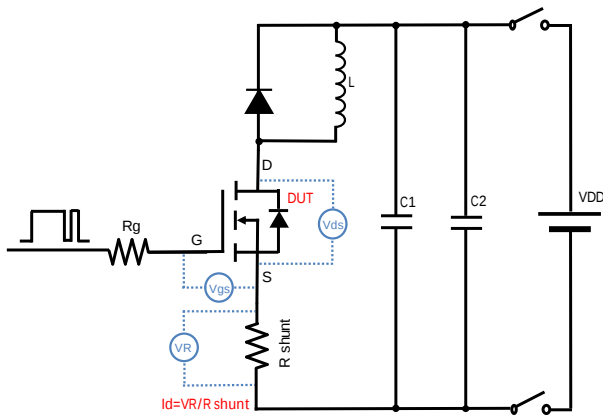


Figure C. Resistive Switching Test Circuit & Waveform

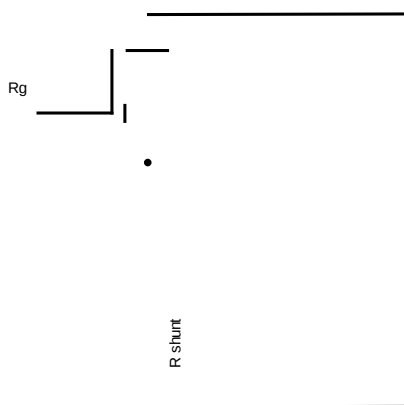
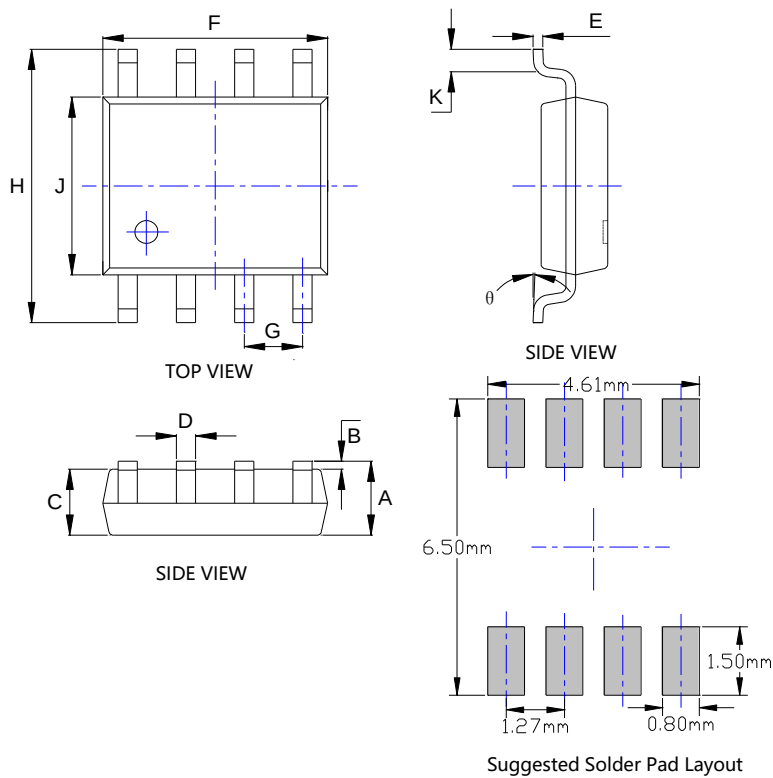


Figure D. Diode Recovery Test Circuit & Waveform



SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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